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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,440	07/18/2003	Kenichi Kawaguchi	60188-536	1018

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McDermott, Will & Emery  
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Washington, DC 20005-3096

EXAMINER

PAN, DANIEL H

ART UNIT	PAPER NUMBER
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2183

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/621,440

Applicant(s)

KAWAGUCHI, KENICHI

Examiner

Daniel Pan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 7 and 8 is/are pending in the application.
- 4a) Of the above claim(s) 1-6,9 and 10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7 and 8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☒ Certified copies of the priority documents have been received in Application No. 09/536,308.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>07/18/03</u> .  | 6) <input type="checkbox"/> Other: _____                          |

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1. Claims 7 and 8 are presented for examination. Claims 1-6,9-10 have been canceled. TD on 10/24/06 has been received.

2. As to claim 7, Claim 7 is objected to because of the following informalities: The word "capable" is not a positive recitation of the limitation. Applicant is suggested to change to more positive language to avoid possible broader reading of the claim. Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Phillips et al. (5,426,743).

3. As to claim 7, Phillips taught at least :

a) instruction register which stored at least two instructions (see not explicitly shown , but see the issuance of ALU instructions for execution in col.2, lines 36-49, see also the general purpose read ports of the register array for LAU1 and ALU2 instructions in col.8, lines 57-67):

b) a decoder which decodes the at least two instructions (see how the CSA reduced the 3 instruction operands to sum and carry in col.3, lines 41-48)

c) a first execution unit (see any of the alu1 in fig.2);

d) a second execution unit (see any other alu2 in fig.2; and

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e) instruction parallelizing/executing/recognizing means (see also gif.2, col.2, lines 1-6) for executing two instructions, which designated the first execution unit (see designated 2-1 ALU) as a target in parallel by allocating one of the at least two instructions to a second execution unit (see 3-1 ALU unit) wherein the instruction parallelizing/executing means was capable of converting one of the two instructions to another instruction that designated at least a second execution unit (see how the second instruction of the pair being executed in an identical machine cycle in parallel with the first instruction by a second ALU , 3-1 ALU, in col.8., lines 55-67, col.9, lines 1-20).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 7,8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eikemeyer et al. (5,355,460) in view of Holmann et al. (5,815,698).

5. As to claims 7,8, Eikemeyer taught :

a) instruction register which stored at least two instructions (see fig.6 [21]):

b) a decoder which decodes the at least two instructions (see detailed decoders in fig.8)

c) a first execution unit (see any of the alu in fig.10);

d) a second execution unit (see any other alu in fig.10; and

e) instruction parallelizing/executing/recognizing means (see fig.1 [11] [12] [16] [13] [14] [15], see also figs.7,8) for executing two instructions, which designated the first

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execution unit (see designated function unit) as a target in parallel by allocating one of the at least two instructions to a second execution unit (see any other function unit) wherein the instruction parallelizing/executing means was capable of changing one of the two instructions to another instruction that designated at least a second execution unit (see how the compound analyzer to determine the capability for parallel execution of the first instruction and second instruction in co1.11, lines 54-68, co1.12, lines 1-44, co1.13, lines 52-68, co1.14, lines 1-10, see also fig.10, co1.15, lines 51-68, co1.16, lines 1-6 for respective execution function units 61,62,63,64 of the instructions, see fig.11 for example of the pair of instructions).

6. As to the newly amended feature of converting one of the two instructions to another instruction designating a second execution unit, Eikemeyer did not specifically show the conversion of the instruction as claimed. However, Holmann taught instructions can be converted to another instruction for execution by an execution unit (see col.2, lines 43-50). It would have been obvious to one of ordinary skill in the art to use Holmann in Eikemeyer for converting the instruction to another instruction for execution as claimed because the use of Holmann could provide Eikemeyer the capability to adapt to different instruction format, and it can be achieved by reconfiguring the conversion format of Holmann into Eikemeyer with added changes in control formats, such as the instruction width, and instruction type, so that specific conversion of Holmann could be recognized by Eikemeyer, and because Eikemeyer also taught a compound instruction analyzer to determine the capability for parallel execution of the first instruction and second instruction in co1.11, lines 54-68, co1.12, lines 1-44, co1.13, lines 52-68, co1.14, lines 1-10) for particular machine (see fig.10, co1.15, lines 51-68, co1.16, lines 1-6 for respective execution function units 61,62,63,64 of the instructions, see fig.11 for example of the pair of instructions), which was a suggestion of the need for converting instruction to another instruction in order to identify the groupings of the instructions to be executed by the respective execution unit, and for the above reason, provided a motivation.

7. The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

a) Scantlin (5,574,927) is cited for the teaching of the parallel execution of the two instructions and decoders with a target processor (see fig.2, fig.3, co1.8, lines 11-65).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***21 Century Strategic Plan***

  
DANIEL H. PAN  
PRIMARY EXAMINER  
2008